GaAs Monolithic MIC Mixer-IF Amplifiers for Direct Broadcast Satellite Receivers.

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ABSTRACT

An MMIC mixer-IF amplifier (MIX-IFA) and a band-pass filter (BPF) have been developed for DBS receiver applications. The MIX-IFA chip with a size of 2.0 x 2.25 mm^2 contains a balanced-type diode mixer using a newly designed 3-dB hybrid circuit and a resistive feedback-type single-stage IF amplifier. The MIX-IFA shows a noise figure of $\leq$ 12 dB and a conversion gain of 1.5 dB for signal frequencies from 11.7 to 12.2 GHz with a minimum noise figure of 9 dB and a maximum conversion gain of 3.5 dB. All the circuit elements such as Schottky diodes, FET and resistors are fabricated in a planar structure by using selective ion-implantation technology for realizing good uniformity and reproducibility. The BPF chip designed from modification of high-pass filter exhibits an insertion loss of $\leq$ 1 dB for signals and an attenuation of $\geq$ 10 dB for images.

With the previously developed LNA, IFA and local oscillator, all MMIC components for DBS receiver are prepared.

1. Introduction

Extensive efforts are being directed in various laboratories[1][2][3] towards the development of GaAs monolithic MICs (MMICs) for application to 12-GHz direct broadcast satellite (DBS) receivers. For such application, we have already demonstrated three kinds of GaAs MMICs; low-noise amplifier, IF amplifier and dielectric resonator oscillator[4].

Various factors have to be traded off for a proper selection of circuit configuration of an MMIC. A mixer, for example, can be realized by using either a dual-gate FET or Schottky diodes[5][6]. Dual-gate FET mixers have better conversion gain and smaller chip size, whereas Schottky diode mixers give lower noise figure and require no DC bias circuitry. Besides these, circuit designability is also very important factor to be considered.

This paper describes an MMIC mixer-IF amplifier (MIX-IFA) and a band-pass filter (BPF) developed for DBS receiver applications. A balanced-type Schottky diode mixer and a single-stage IF amplifier are incorporated into the MIX-IFA chip, where a compact 3-dB hybrid circuit is used in the mixer for chip size reduction and a direct impedance match is realized between the mixer and the IF amplifier. the BPF chip has been designed modifying a high-pass filter. Selective ion-implantation technology has been used throughout to make the Schottky diodes, FET and resistors in a planar structure for good uniformity and reproducibility. Circuit design, device fabrication and RF performance of the MIX-IFA are described in the following sections, and, finally, design and performance of the BPF are mentioned.

2. Circuit Design of Mixer-IF Amplifier

In terms of circuit designability, noise figure, impedance match and simplicity of DC circuitry, a balanced Schottky diode mixer has been selected as a circuit configuration. The drawbacks of balanced diode mixers come from lack of conversion gain and large chip size due to conventional 3-dB hybrids. In order to compensate for these drawbacks, a new type of compact 3-dB hybrid has been adopted, and, moreover, the direct connection of mixer and IF pre-amplifier has been realized in a single chip.

2.1 Mixer Circuit

3-dB hybrid circuits conventionally used in balanced-type mixers, such as rat-race rings, branch-line couplers and interdigitated couplers are inherently distributed circuits, and they require a large pattern area. For chip size reduction, we have designed a new type of balanced mixer using a compact 3-dB hybrid.

The circuit configuration of the designed balanced mixer is shown in Fig.1, where V_S and V_L represent the voltages applied to signal and local ports, respectively, and V_{D1} and V_{D2} the terminal voltages of the diodes due to V_S and V_L.
Now let us assume that the hybrid circuit satisfies the following equation:

$$\begin{bmatrix} V_1 \\ I_1 \end{bmatrix} = \begin{bmatrix} -1 & 0 \\ 0 & -1 \end{bmatrix} \begin{bmatrix} V_2 \\ I_2 \end{bmatrix} , \qquad (1)$$

where V_1 and V_2 are the voltages appearing across each port of the hybrid, and I_1 and I_2 are the currents flowing into and out of the ports. Moreover, let us assume here that the both diodes have the same impedance for the signal and local frequencies, respectively. Then it can be shown that V_{D1}'s and V_{D2}'s corresponding to $V_S(\omega_S)$ and $V_L(\omega_L)$ satisfy

$$V_{D1}(\omega_S) = V_{D2}(\omega_S) = V_S(\omega_S), \qquad (2)$$

and

$$V_{D1}(\omega_L) = -V_{D2}(\omega_L) = -V_L(\omega_L), \qquad (3)$$

where ω_S and ω_S denote the signal and local angular frequencies, respectively. Hence the circuit in Fig.1 can operate as a balanced mixer. The hybrid circuit satisfying (1) is equvalent to a 180° phase-shift circuit.

The balanced mixer with such circuit configuration has been designed, and its equivalent

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circuit is shown in Fig.2. The 180° hybrid circuit is realized with three series-connected high-impedance transmission lines (T_{L1}, T_{L2} and T_{L3}), and two shunt-connected capacitors (C_1 and C_2) of an interdigitated type. These elements have been optimized for a local frequency of 10.7 GHz by a computer simulation. T_{L1}, T_{L2} and T_{L3} have a characteristic impedance of 95 Ω and line lengths of 0.09 λ_g, 0.18 λ_g and 0.09 λ_g, respectively, where λ_g is the guided wavelength for the local frequency of 10.7 GHz. The values of C_1 and C_2 are 0.14 pF.
The amplitude and phase imbalances between the diode terminal voltages have been calculated to be less than ±0.5 dB and ±10°, respectively, for both the signal and the local. The isolation between the signal and local ports is greater than 20 dB, over a relative bandwidth of 12 % around the center frequency.

Transmission lines T_{L4} and T_{L5} are for signal impedance matching, and T_{L6} and T_{L7} for local impedance matching. The IF signal is taken out through T_{L4} which is short-circuited RF-wise at the IF port by series-resonant L_1 and C_4.
The shorted stub T_{L7} is used for the IF signal return.

2.2 Schottky Diode

Figure 3 shows the top and cross-sectional schematics of Schottky diode used. Aluminum is employed as the Schottky barrier metal. In order to protect the aluminum electrode from migration due to a rectified current, an interdigitated structure has been adopted so as to reduce the unit electrode finger length, w_{DG}, to 5 μm.
The length of Schottky electrode, L_{DG}, is made to be 1 μm which is identical to the gate length of the FET used in the IF amplifier described later. The total effective electrode width or the total effective finger length, W_{DG}, and the active layer parameters have been determined by a computer simulation in terms of conversion loss, local power, and diode reflection coefficients with respect to 50 Ω for signal, local and IF frequencies. Using the ideality factor n(=1.25) measured beforehand, diode DC parameters such as saturation current I_S, series resistance r_S and junction capacitance C_j have been calculated using a one-dimmensional model of the diode. RF characteristics such as conversion loss L_C, optimum local power $P_{LO,opt}$, rectified current I_D for $P_{LO,opt}$ and reflection coefficients Γ_S, Γ_{LO} and Γ_{IF} for signal, local and IF frequencies have been calculated by a nonlinear analysis(7).
By taking into account these computer-simulated results and also the fabrication process, the carrier concentration and the thickness of diode active layer have been determined to be $1.0 \times 10^{17}cm^{-2}$ and 0.2 μm, respectively.

Figure 4 shows the calculated dependence of $P_{LO,opt}$, I_D and $|\Gamma_{LO}|$ on the total electrode width W_{DG} for signal frequency f_S=12 GHz and local frequency f_{LO}=10.7 GHz. With an increase of W_{DG}, $P_{LO,opt}$ and I_D increase, while $|\Gamma_{LO}|$ decreases.
For a local power of 5.5 dBm, W_{DG} can be determined from Fig.4 to be 30 μm. Hence each diode has been designed for the electrode width of 15 μm, where the number of fingers, N, is 3 for the unit finger length w_{DG} of 5 μm. Using these diode parameters, r_S, C_J and I_S are calculated to be 31 Ω, 0.06 pF and 4×10^{-12}A, respectively. The calculated conversion loss L_C is 4.5 dB for a local power of 5.5 dBm, and Γ_S, Γ_{LO} and Γ_{IF} are found to be $0.51\angle -16°$, $0.60\angle -20°$ and $0.76\angle -2°$, respectively, when IF frequency (=f_S- f_{LO}) is 1.3 GHz.

2.3 Mixer-IF Amplifier (MIX-IFA)

The equivalent circuit of MIX-IFA is shown in Fig.5. Since the IFA is required to operate over a wide frequency range of 0.5-1.5 GHz, a single-stage FET amplifier with resistive feedback has been designed. The IFA is directly connected to the mixer IF output port through a spiral inductor L_2 and DC-block capacitor C_5. The source resistor R_S and the bypass capacitor C_S are incorporated for single power-supply operation. The drain resistor R_D and the bypass capacitor C_D connected to the drain terminal act as an RC filter, thus eliminating the RF choke otherwise necessary outside the chip. The gate resistor R_G is used to lower the input VSWR. The gate length and width of FET are 1 μm and 800 μm, respectively. By using a computer simulation, the gate width, L_2, R_G, R_D and the feedback resistor R_F have been optimized in terms of noise figure, gain flatness, input impedance and output VSWR.

3. Device Fabrication

Figure 6 shows the MIX-IFA chip with a size of 2.0 x 2.25 mm^2 and a thickness Of 0.3 mm.
The mixer diodes, FET and resistors have been fabricated by selective Si ion implantation into an undoped semi-insulating GaAs substrate.
A resist/SiO_2 film is used as a mask for the ion implantation. The active layers have been formed under an accelaration energy and a dose of 220 keV and $5 \times 10^{12}cm^{-2}$ for mixer diodes, and 70 keV and $3.5 \times 10^{12}cm^{-2}$ for the FET, respectively.
For the n^+ contact layers and resistor layers, Si ions are dually implanted with energies of 120 keV and 250 keV and a dose of $2 \times 10^{13}cm^{-2}$.
After ion implantation and removal of the resist/SiO_2 film, the wafers were annealed at 850 ℃ for 15 minutes in AsH_3/Ar atmosphere without encapsulants.

The Schottky Barrier electrodes were formed by Al with a thickness of 6000 Å. The ohmic electrodes were formed by alloying Pt/AuGe evaporated on the n^+ layers at 450 ℃. The first level metallization of the MIM capacitors is 0.8 μm thick aluminum.
A plasma CVD Si_3N_4 film with a thickness of 2000 Å is used as the capacitor dielectric.
The Au/Pt/Ti metal system is used for the top plates of the capacitors, spiral inductor, the bonding pads and the interconnection metal.
All of the metal patterns were formed by a lift-off process.

After lapping the substrate to a thickness of 300 μm, the backside of the wafer was metalized.

4. RF Performance

4.1 Balanced Diode Mixer

In order to diagnose the MIX-IFA the individual MMICs of mixer and IFA have been fabricated in the same wafer.

Figure 7 shows the measured frequency response of return losses at the signal and local ports. A signal port VSWR of $\leq$ 2.0 has been obtained at frequencies from 10.9 to 12.9 GHz. The optimum for local port VSWR has been achieved at ~ 10.2 GHz which is lower than the design center frequency of 10.7 GHz. The discrepancy is most likely caused by the fact that the interdigitated capacitor used in the 3-dB hybrid was assumed to be a pure lumped element in the hybrid circuit design. The actual interdigitated capacitor, however, is found to differ from the lumped element design due to the distributed effect of its finger electrode.

Figure 8 shows the measured local power dependence of mixer conversion loss at f_{LO}=10.7 GHz and 10.2 GHz. The minimum conversion loss is 8.5 dB at f_{LO}=10.2 GHz and P_{LO}=7 dBm. For f_{LO}=10.7 GHz, however, the minimum conversion loss is 8 dB at P_{LO}=13 dBm.

4.2 IF Amplifier (IFA)

Figure 9 shows the measured frequency response of gain and noise figure of the IFA chip at V_{DD}=8V and I_{DD}=15 mA. A gain of $\geq$ 10 dB and a noise figure of $\leq$ 3 dB have been obtained at frequencies from 0.5 to 1.3 GHz.

4.3 Mixer-IF Amplifier (MIX-IFA)

Figure 10 shows the measured local power dependence of conversion gain G_C and noise figure NF for f_{LO}=10.2 GHz and 10.7 GHz. For f_{LO}=10.2 GHz, a minimum noise figure NF_{min}=11.5 dB and G_C=-1.0 dB have been obtained at P_{LO}=7 dBm. For f_{LO}=10.7 GHz, NF_{min}=10 dB and G_C=2.0 dB have been obtained at P_{LO}=13 dBm.

Figure 11 shows the measured frequency response of conversion gain and noise figure at f_{LO}=10.7 GHz and P_{LO}=13 dBm. $G_C \geq$ 1.5 dB and NF $\leq$ 12 dB have been obtained at frequencies from 11.7 to 12.2 GHz. The minimum noise figure and the maximum conversion gain are 9 dB and 3.5 dB, respectively, at 11.5 GHz.

The local to IF port, signal to IF port and local to signal port isolations have been measured to be 40 dB, 28 dB and 35 dB, respectively. The IF output port VSWR has been found $\leq$ 1.6 for 1.0-1.3 GHz and $\leq$ 2.0 for 0.4-1.6 GHz.

5. Band-Pass Filter (BPF)

Figure 12 shows the equivalent circuit and the top view of the BPF chip fabricated on GaAs. In the BPF design, it was aimed to minimize the insertion loss for signal frequencies from 11.7 GHz to 12.2 GHz and to obtain an attenuation of $\geq$ 10 dB for image frequencies of from 9.2 to 9.7 GHz. For chip size reduction, a modified high-pass filter is adopted that consists of two series-connected capacitors, C_{S1} and C_{S2}, and shunt-connected high-impedance line T_L terminated by a capacitor C_P. All the capacitors are of an interdigitated structure, and have been fabricated with an accuracy of $\leq$ 5 %. The chip has a size of 1.5 x 1.25 mm^2, and its thickness is 0.3 mm.

Figure 13 compares the measured performances of the BPF with the calculated ones. An insertion loss of $\leq$ 1 dB and VSWR of $\leq$ 1.5 have been obtained at frequencies from 11.7 to 12.2 GHz. At image frequencies from 9.2 to 9.7 GHz, an attenuation of $\geq$ 10 dB has been obtained. The agreement between the measured and the calculated is relatively good.

6. Conclusion

It has been shown that the developed mixer-IF amplifier has a noise figure of $\leq$ 12 dB and a conversion gain of $\geq$ 1.5 dB for 11.7-12.2 GHz signal frequencies at a local power of 13 dBm. Improvement of noise figure down to 8 dB as well as reduction of local power down to 8 dBm can be expected from further optimization of the 3-dB hybrid.

The present work has revealed that the balanced mixer configuration using the newly designed 3-dB hybrid and the direct mixer-IF amplifier combination offer a useful means for reducing chip size yet with good circuit designability. The MMICs presented in this paper, together with the previously reported ones[4], have paved the way to all-MMIC DBS receivers.

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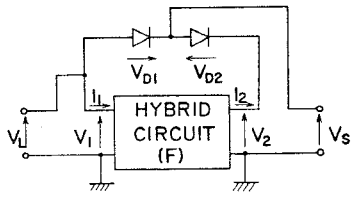

Fig. 1 Circuit configuration of balanced diode mixer.

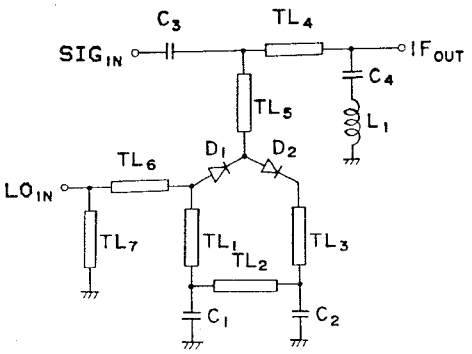

Fig. 2 Equivalent circuit of diode mixer.

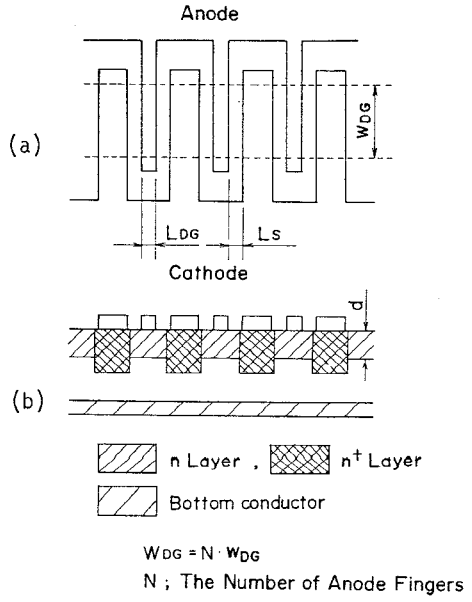

Fig. 3 (a) Top and (b) cross-sectional schematics of Schottky diode.

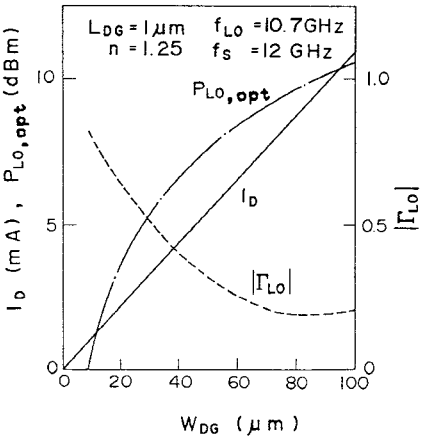

Fig. 4 Calculated $P_{LO,opt}$, I_D and $|\Gamma_{LO}|$ as a function of total electrode width W_{DG}.

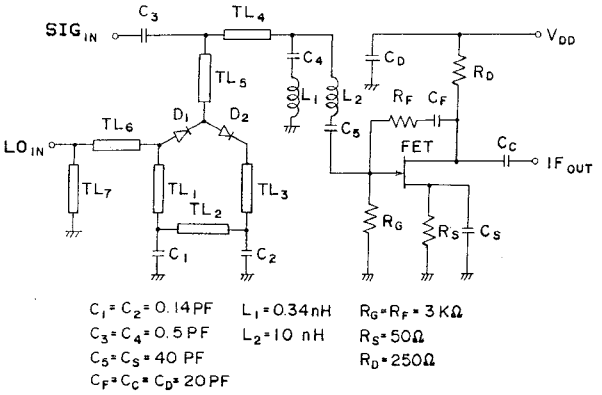

Fig. 5 Equivalent circuit of MIX-IFA.

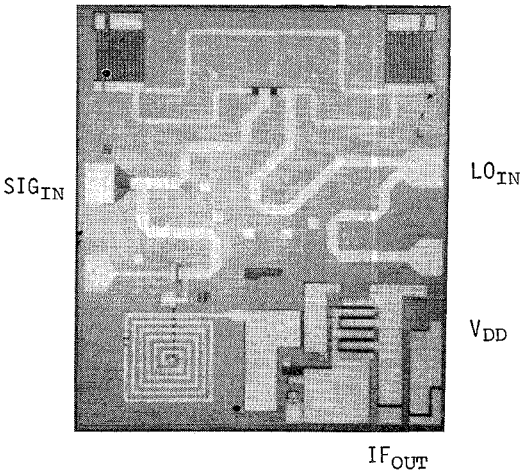

Fig. 6 MIX-IFA chip (2.0 x 2.25 mm^2).

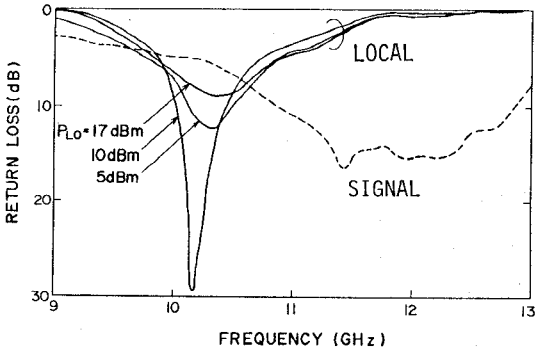

Fig. 7 Measured return losses of mixer as a function of frequency.

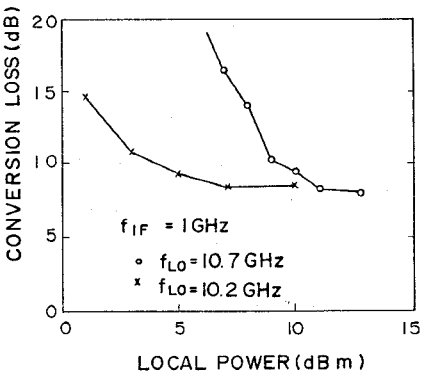

Fig. 8 Measured conversion losses of mixer as a function of local power.

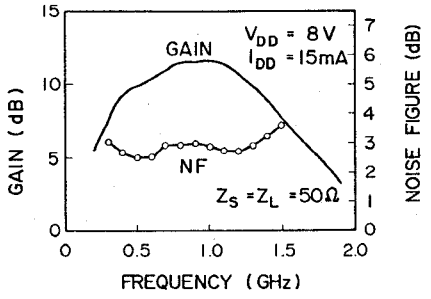

Fig. 9 Measured gain and noise figure of IFA as a function of frequency.

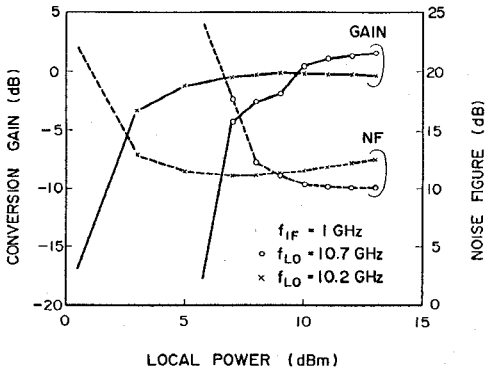

Fig. 10 Measured conversion gain and NF of MIX-IFA as a function of local power.

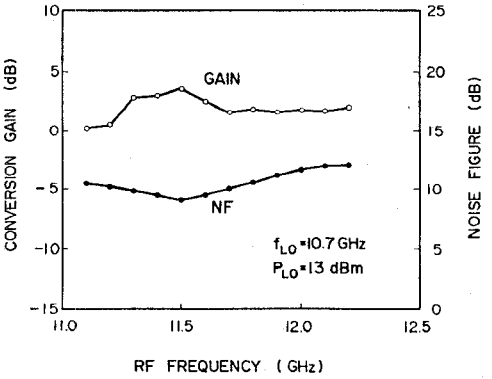

Fig. 11 Measured conversion gain and NF of MIX-IFA as a function of RF signal frequency.

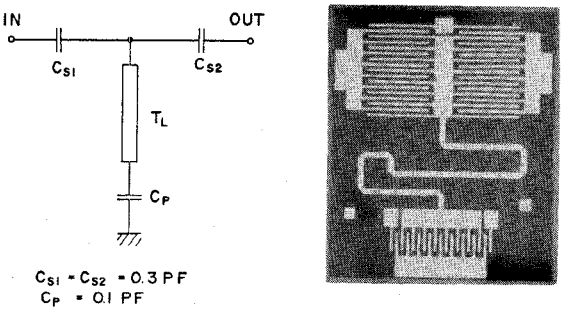

Fig. 12 (a) Equivalent circuit of BPF and (b) BPF chip (1.5 x 1.25 mm^2).

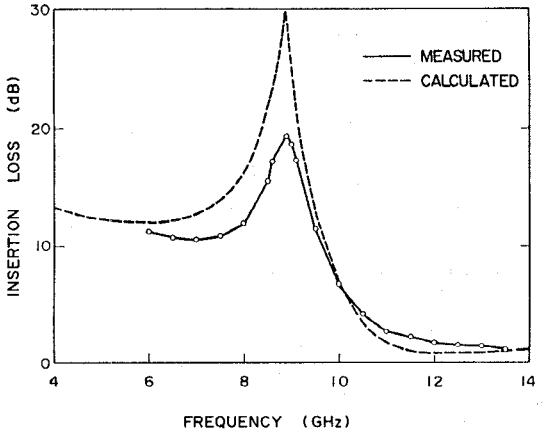

Fig. 13 Measured and calculated frequency responses of BPF.